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Suitable Codes Design for Frequency Offset Correction and Channel Matched Filter in HIPERLAN

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ABSTRACT: Frequency offset can introduce considerable difficulties in both the training and detection of an equaliser based system. In the ETSI HIPERLAN (High PERformance Radio LAN) standard, the oscillators are specified to be within 10 ppm. Obviously, the residual frequency offset in the received baseband signal can seriously affect the final performance of the system. In this paper, we present the design of suitable frequency offset correction and synchronisation codes. These codes are then applied to a CMF (Channel Matched Filter) structure which is followed by a low complexity DFE implementation based on the zero forcing algorithm. The performance of such a receiver is analysed for the Hiperlan scenario and then compared with that obtained from a DFE using the LMS algorithm.

I-INTRODUCTION

The ETSI Hiperlan standard operates at 5.2 GHz and supports instantaneous bit rates of just under 24 Mb/s. This system is defined to meet the increasing need for high capacity indoor wireless applications. In Europe, 150 MHz of dedicated spectrum has been allocated to this system. The Hiperlan physical layer uses GMSK combined with adaptive equalisation to overcome the harmful effects of Inter-Symbol Interference (ISI), however the exact form of equalisation is not specialised in the standard [1].

The ISI introduced by delay spread has a considerable impact on the choice of air interface technique [2]. Over the years there have been many different techniques developed to combat this problem, these include adaptive equalisation, direct sequence and frequency hopped CDMA, COFDM and various multicarrier architecture. For Hiperlan, adaptive equalisation was studied and chosen as the most appropriate choice for overcoming the severe ISI effects introduced by the radio channel. [3]

In any practical Hiperlan receiver there is a need for carrier and frame synchronisation. Due to the packet based nature of the transmission and the limited frequency stability of the transmit and receiver oscillators, without compensation there will be a residual frequency offset in the received baseband signal. Such an offset will prevent the equaliser from working effectively. This problem can be solved by using a complex correlator to generate two or more time spread phase estimates. In this paper, we propose a new training sequence structure and discuss its practical performance. The codes have been carefully designed for both synchronisation and frequency offset correction. We also

analyse the system performance based on the use of a Channel Matched Filter (CMF) combined with a zero forced DFE structure. This system has been proposed to minimise the computational complexity of the adaptive equalisation training process.

II-HIPERLAN PHYSICAL LAYER AND CHANNEL MODEL

The Hiperlan physical layer includes a digital modem, channel coding and equaliser. Constant envelope modulation schemes such as Gaussian Minimum Shift Keying (GMSK) were considered as the most appropriate choice for achieving the transceiver linearity requirements, spectral efficiency and equaliser complexity targets. For Hiperlan, a BT product of 0.3 was chosen to optimise the bit rate in a fixed bandwidth [2]. Pre-coding techniques are used to remove the differential aspects of the GMSK modulation scheme [4] in order to improve BER performance and eliminate state resetting before insertion of the channel sounding sequence.

A high rate (31, 26) BCH code with interleaving has been chosen for Hiperlan. This channel coding scheme can be used to significantly improve the number of error-free packets (i.e. the packet outage probability) but cannot necessarily improve the average BER performance [2].

A full investigation into the Hiperlan radio channel and its impact on equalisation is given in [5]. In our simulation, an N ray model ($N = 8$) is used as the basis for generating each of the 11 T-spaced samples of the delay profile with rms delay spreads up to 150 ns.

Equalisation was used for ISI compensation, however a single equaliser is not always sufficient to handle the channel. Diversity techniques have been proposed for those areas where robust, high quality reception is required. [2][6]

III-SYNCHRONISATION CONSIDERATION

Synchronisation, which includes symbol clock, frame and carrier synchronisation, has to be considered carefully. A free-running clock can be used for symbol timing since a DFE with fractional-spacing in the feedforward section is not sensitive to sampling phase. If there is any frequency offset between the local clock and the clock of the incoming signal, the optimum sampling point will drift. If it is defined that $\Delta\tau / T < 0.2$ is acceptable, where $\Delta\tau$ is the drift in the sampling instant over one symbol period, then

the maximum tolerable clock frequency offset, denoted by Δf_b , is given in equation 1.

$$\Delta f_b = \frac{1}{NT} \times \frac{\Delta \tau}{T} \quad (1)$$

where N is the number of bits in the longest packet and T is the bit period. Assuming the transmission of a packet containing a maximum of 23,762 bits (based on GMSK at a bit rate of 24 Mbits/s), from equation 1 the maximum tolerable clock frequency offset is 198 Hz. Therefore, the clock frequency stability at both the transmitter and receiver should be ± 99 Hz around a clock frequency of f_b (24 MHz), this requires a clock frequency stability $\Delta f_b / f_b$ of over 4 ppm which can be achieved using a low cost quartz oscillator. Hence a free running clock can be used for the clock frequency generation.

Frame synchronisation is important since it affects the equaliser training performance. The Hiperlan frame structure includes a synchronisation and training sequence made up of 450 bits. In our system design, the start of the synchronisation sequence is used to acquire frame synchronisation, this information is then passed to the equaliser and training then begins. If the frame acquisition uses a large number of bits, the resulting data may not be sufficient to converge the equaliser's coefficients. This problem is particularly important if the LMS algorithm is used to obtain the equaliser's coefficients.

PN (PseudoNoise) sequences are classically used for frame synchronisation, but the synchronisation sequences will not only be used to identify the synchronisation of the training sequence but also the channel impulse response [7]. This is the case especially in a CMF implementation. The aperiodic ACF (Auto-Correlation Function) properties are affected by the random data and noise. Accurate estimation of the impulse response of the channel results in a need to minimise the ACF side-lobe levels. Carrier synchronisation is related to the frequency offset problem and discussed in the following section.

IV-FREQUENCY OFFSET IN HIPERLAN

For Hiperlan, one of the most important considerations at the receiver is the compensation for frequency offset. Due to the limited frequency stability of the transmit and receive oscillators, without compensation there will be a residual frequency offset in the received baseband signal.

The presence of carrier offset will cause a constant rotation of the carrier phase, resulting in a time-variant channel. If the phase rotation within a packet caused by carrier frequency offset is small, say less than 20 degrees, the channel can be reasonably regarded as static. The maximum frequency offset tolerable under this condition can be calculated very easily from equation (1),

$$\Delta f_c = \frac{1}{NT} \times \frac{20^\circ}{360^\circ} \quad (2)$$

GMSK with a bit rate of 24Mbits/s and a maximum packet length of 23,762 bits will result in a maximum tolerable frequency offset of around 56 Hz (based on equation 2).

The frequency stability at both the Tx and Rx should be within ± 28 Hz around a carrier frequency f_c of 5.2 GHz, this requires a frequency stability of 0.0052 ppm. This value is obviously impractical and hence methods for combating carrier offset are important in the transceiver design.

In the Hiperlan standard, the oscillators are specified to be within 10ppm, hence the worst case frequency offset will be 104 kHz. The presence of such carrier frequency offsets is undesirable since it will cause variations in the channel characteristics. Consequently, the coefficients resulting from the initial training will not be valid for equalising the subsequent data, especially for long packets where the signal phase can rotate significantly.

One compensation method is to use a data derived technique to generate an error signal which is then passed through a PLL (Phase Locked Loop) during DFE training as shown in Figure 1. This approach is good for small values of frequency offset (say 10 kHz) but is limited to operation after the equaliser training process (since the channel ISI would distort the process). Assuming derived phase recovery is applied after the initial training process, equation 2 could be modified such that N represents the training sequence length (say 450 bits). The training algorithm can tolerate a limited amount of phase rotation across the training sequence, for a value of 20 degrees this would result in the initial frequency offset estimate having to be with 2.94 kHz of the nominal carrier frequency.

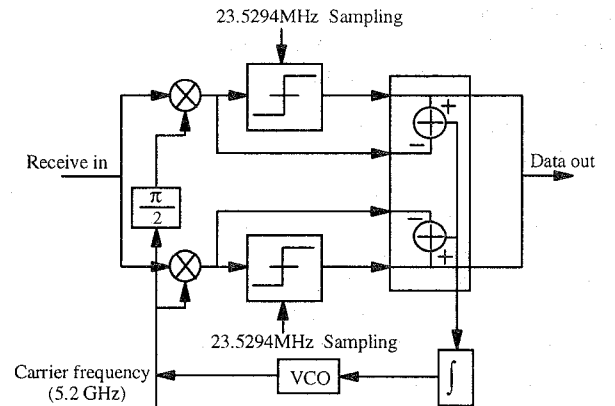


Figure 1: Data Derived Technique for Frequency Offset

The solution presented in the paper allows large frequency offsets to be compensated and is based upon an initial coarse frequency offset compensation technique. Instantaneous channel phase can be measured using the I and Q outputs of the matched filter. By sending the synchronisation sequence repeatedly at the start of the frame, channel phase variations during the interval of two successive synchronisation sequences can be measured and the coarse frequency offset derived and subsequently removed.

The matched filter generates a channel characteristic in a complex I and Q form after receiving the transmitted synchronisation sequence as

$$h(t) = h_i(t) + j h_q(t) \quad (3)$$

If the radio channel is assumed static, any phase rotation of the receiver can be attributed to carrier frequency offset. The matched filter output at the receiver for the next synchronisation sequence is given by:

$$h'(t) = e^{j2\pi\Delta f_c NT} [h_i(t) + j h_q(t)] \quad (4)$$

where N is the number of symbols between two synchronisation sequences and T is the symbol period, Δf_c is the carrier frequency offset. Clearly, the power delay profile is independent of frequency offset (hence it is the phase and not the magnitude of the equaliser taps that needs adjusting). To minimise noise effects, the peak of the channel power delay profile can be used as the reference point when measuring the channel phase rotation. If the measured phase rotation is denoted by $\Delta\theta$, the frequency offset can be calculated by $\Delta f_c = \Delta\theta / 2\pi NT$. The synchronisation sequence insertion rate should be at least twice as high as the maximum frequency offset to be compensated. This will guarantee that the maximum phase rotation between the two synchronisation sequences will be less than 180° in order to avoid phase and frequency ambiguity.

The compensation technique for a practical Hiperlan system has to consider that the frequency offset varies between 0 and 104 kHz and we must bear in mind that no delaying or buffering can be used in a Hiperlan system. This differs from the technique in [7], which was successful in the ESPRIT LAURA (Local Area User Radio Access) project but does not meet Hiperlan specifications.

TRAINING SEQUENCE CODE DESIGN

Codes have been carefully designed as 32 bit complex sequences, these give sufficient processing gain for synchronisation in the system. The transmission rate is 24 Mb/s (i.e., a bit period of 42 ns). The maximum rms delay spread that the system will encounter is assumed to be 150 ns. Hence the ACF of the synchronisation sequence would have to have low side-lobe levels for approximately 5 bit periods either side of the peak. The sequence has the following auto- $[R(n)]$ and cross- $[C(n)]$ correlation properties at $n=0,1,2,\dots,9,10$:

$$R(n) = \begin{cases} 1, & n = 0, \\ 0, & n = \pm 1, \pm 2, \dots, \pm 10 \end{cases} \quad (5)$$

$$C(n) = 0, \quad n = 0, \pm 1, \pm 2, \dots, \pm 10 \quad (6)$$

Table 1 list some examples of the best sequences found. All these sequences have a length of 32 bits, resulting in two 16 bits staggered sequences on the I and Q channels after GMSK modulation.

| No. | Input Binary sequence to pre-coded GMSK |
|-----|---|
| 1 | 10010100111111100101001100000001 |
| 2 | 11111011001011110111111001001001 |
| 3 | 00100101110011010000101001101010 |
| 4 | 10001011010110000100111011111011 |
| 5 | 01000010111010011011001110000001 |

Table 1: Examples of Synchronisation Sequences with desired auto- and cross- correlation for Hiperlan

The design codes are part of a PN sequence, the ACF (Auto-correlation Function) property of the first sequence is shown in Figure 2 as an example. With the padding bits (10), it gives a total sequence length of 52 bits. The total length of the sequence is not important since we simply use the 32 bits in the complex auto-correlation process.

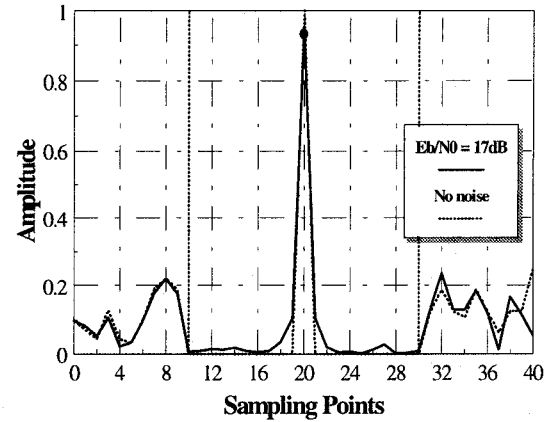


Figure 2: The ACF property of the designed codes

The training sequence has been designed and given in [1]. The length of the sequence is 450 bits as mentioned above. In our design, in order to measure the frequency offset, we have to change the original structure to produce a new sequence where we insert 5 sets of design codes at the beginning of the training sequence. Figure 3 illustrates these changes and shows the signal format of a typical data packet compared with the top one which is the standard Hiperlan frame structure.

The packet begins with 450 bits as a training sequence. In the structure of the training sequence, we insert 10 bits for padding and then follow this with five sets of 32 bit sequences. The first 32 bits are used for synchronisation and channel estimation. All five 32 bit sets are used for the measurement of frequency offset, whose information can be derived based upon the phase of the correlation results. This kind of measurement is still affected by noise, this has been measured in an AWGN channel with 17 dB Eb/No and the resulting phase error was approximately 4.5° . The resulting residual frequency offset after coarse compensation would be approximately 2.3 kHz, based on our earlier estimations, this value is within the range required for equaliser training.

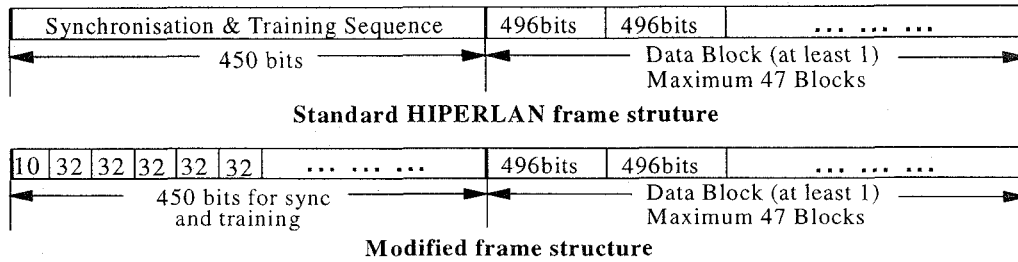


Figure 3: The Signal Format of a Input Packet

The range of frequency offset that can be measured by such a structure lies between 2.3kHz (4.5 degrees after 128 bits) and 358.5 kHz (175.5 degrees after 32 bits). The equaliser training can begin after the first 32 bits have been received and processed. The training sequence length can be as long as 400 bits and this is expected to be enough for the LMS algorithm. Data packets each with 496 bits follow the training sequence.

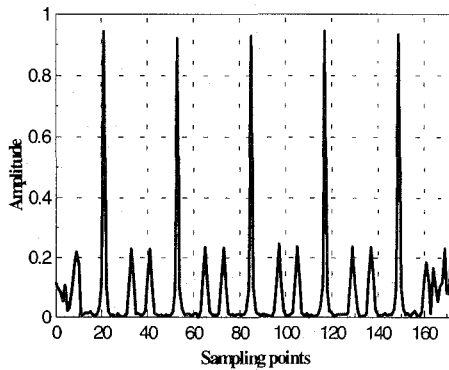


Figure 4: The ACF property of training sequence

The ACF property of the five sets of 32 bit sequences is shown in Figure 4. Its application is shown in [6] and the results we present here are given in Figure 5, which is based on pre-coded GMSK (BT = 0.3) and an rms delay spread of 100 ns. A BCH(31, 26) block code is used and a value of 17dB is assumed for cochannel interference.

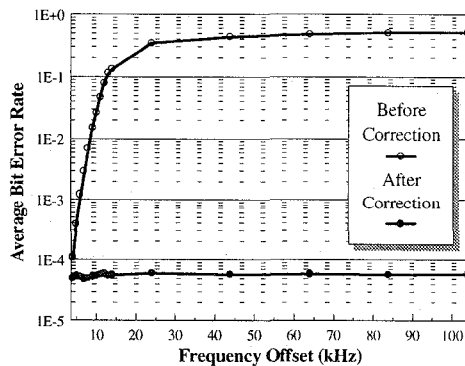


Figure 5: Performance comparison (minimum packet size)

V-CHANNEL MATCHED FILTER IN EQUALISATION

The basic idea of the CMF [8] is to estimate the CIR (Channel Impulse Response) and use it to initialise the

matched filter weights by the time reversed and complex conjugated CIR. If it is ideally matched, the composite impulse response of the matched filter and channel filter model has a purely real central component. The advantage is to reduce the sensitivity to symbol timing error and also to transform a non-minimum phase CIR into a more favourable mixed phase response[9].

The DFE structure for ISI cancellation can be used just after the CMF and the coefficients of the equaliser can be calculated by an iterative algorithm or, more simply, by a direct calculation method based on a zero-forcing algorithm [10]. Figure 6 shows this CMF method used in equalisation. In this example the channel profile is assumed to have 3 taps spaced at the bit period.

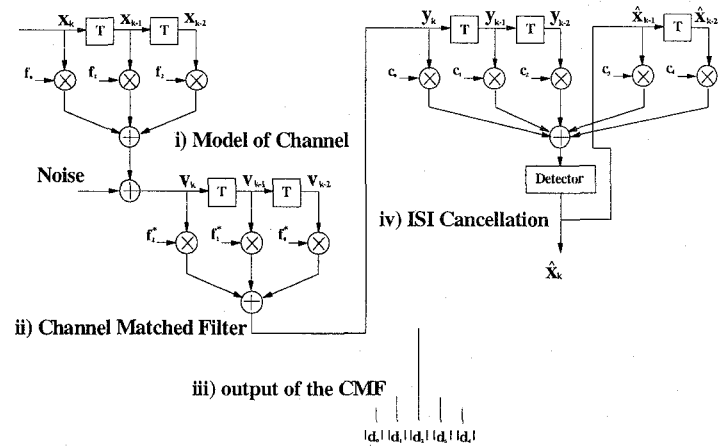


Figure 6: CMF in Equalisation

The ISI components d_i after the CMF are given by

$$\begin{aligned} d_0 &= f_0 f_2^* \\ d_1 &= f_0 f_1^* + f_1 f_2^* \\ d_2 &= f_0 f_0^* + f_1 f_1^* + f_2 f_2^* \\ d_3 &= f_1 f_0^* + f_2 f_1^* \\ d_4 &= f_2 f_0^* \end{aligned} \quad (7)$$

The output of the ISI cancellation is shown in equation 6, where the number of feedforward filter taps is 3 and the number of feedback filter taps is 2.

$$\hat{x}_k = \sum_{i=0}^2 c_i y_{k-i} + \sum_{j=3}^4 c_j \hat{x}_{k-j+2} \quad (8)$$

The coefficients of the DFE can be calculated by:

$$\begin{bmatrix} d_2 & d_1 & d_0 & 0 & 0 \\ d_3 & d_2 & d_1 & 0 & 0 \\ d_4 & d_3 & d_2 & 0 & 0 \\ 0 & d_4 & d_3 & 1 & 0 \\ 0 & 0 & d_4 & 0 & 1 \end{bmatrix} \begin{bmatrix} c_0 \\ c_1 \\ c_2 \\ c_3 \\ c_4 \end{bmatrix} = \begin{bmatrix} 0 \\ 0 \\ 1 \\ 0 \\ 0 \end{bmatrix} \quad (9)$$

The inverse matrix operation in equation 9 can be realised by using a Gauss-elimination type algorithm[11]. For Hiperlan, the Levinson-Durbin algorithm is proposed in order to meet the speed and complexity requirements[12]. For comparison, the LMS algorithm needs $2N+2$ complex operations per iteration (i.e. $400 \times (2N+2)$ for a 400 bit long training sequence) but the whole number of operations for updating by the CMF technique is less than $O(N^2)$, where N is the number of taps in the feedforward filter.

According to the method discussed above, the channel model has been extended to 11 taps and the number of equaliser coefficients to 21 taps. It can be seen that a channel sounding sequence is very important in the estimation of the CIR. The design codes described earlier offer this kind of estimation. Figure 7 shows the results obtained for the Hiperlan system after applying the CMF and DFE (with coefficients computed via block inversion). The graphs show that the performance of the block inversion CMF-DFE is superior to the conventional LMS based iteratively training DFE. In addition to offering lower error floors in the presence of ISI, the CMF block inversion technique also offers at least 3-4 dB of improvement at a BER of 1 in 1000.

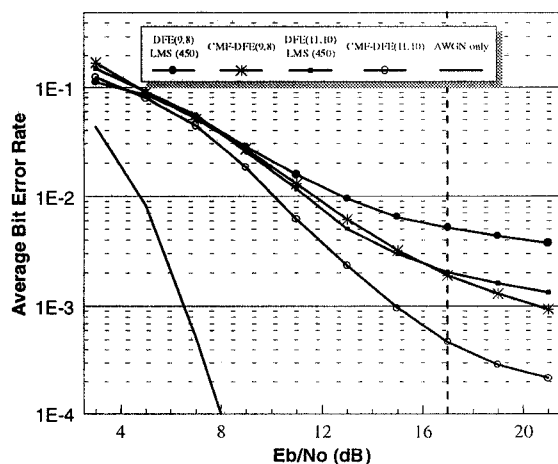


Figure 7: BER performance of CMF-DFE

VI-CONCLUSION

In this paper we have designed a new code sequence and proposed a new structure for Hiperlan training. This structure can also be used to compensate for the effects of frequency offset. It has been shown that the training of the equaliser can start after receiving the first 32 bits. The frequency offset can also be measured over the next four 32 bit sequences. This method has four advantages: (1) it

avoids any buffering; (2) it avoids the ambiguity between small and large values of frequency offset; (3) a large range (from 2.3 kHz to 358.5 kHz) of frequency offset can be measured; (4) average values can be obtained for small frequency offsets. The CMF method based on these codes for the estimation of the CIR in combination with a zero-forced DFE structure offers good performance. When compared with the traditional LMS solution, our approach offers higher performance and a far simpler method for obtaining the DFE coefficients with the number of operations being reduced by up to two orders of magnitude. If this inversion process is based on the Levinson-Durbin algorithm, the complexity can be further reduced [12].

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